1. A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

thereafter simulating said built-in self-test circuit and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said input address and data and said memory address and data are compared in said built-in self-test circuit and a fault output is generated if not matching; and

comparing said fault output and said set of faults to verify the performance of said built-in self-test circuit.

2. The method according to Claim 1 wherein said set of faults comprises an expected faults database file.

3. The method according to Claim 1 wherein said high-level language comprises one of the group of: VHDL and Verilog.

4. The method according to Claim 1 wherein said set of faults comprise any of the group of: stuck at zero and stuck at one.

5. The method according to Claim 1 wherein said built-in self-test circuit performs any algorithm of the group comprising: March C+, Checkerboard, March A, March B, Diagonal, and Walking 0/1.

6. The method according to Claim 1 wherein said step of simulating further comprises:

scrambling said input data and address patterns prior to input into said embedded memory behavior model; and

de-scrambling said memory address and data prior to said comparing of said input address and data and said memory address and data in said built-in self-test circuit.

7. The method according to Claim 1 further comprising de-scrambling said set of faults prior to said step of comparing said fault output and said set of faults.

8. A method to verify the performance of a built-in self-test circuit for testing embedded memory in an integrated circuit device comprising:

introducing a set of faults into an embedded memory

behavior model wherein said embedded memory behavior model comprises a high-level language model and wherein each member of said set of faults comprises a finite state machine state, a memory address, and a memory data fault;

thereafter simulating said built-in self-test circuit and said embedded memory behavior model wherein said built-in self-test circuit generates input data and address patterns for said embedded memory behavior model, wherein said input data and address patterns are scrambled prior to input into said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are de-scrambled and then are compared to said input address and data in said built-in self-test circuit and a fault output is generated if not matching;

de-scrambling said set of faults; and

thereafter comparing said fault output and said set of faults to verify the performance of said built-in self-test circuit.

9. The method according to Claim 8 wherein said set of faults comprises an expected faults database file.

10. The method according to Claim 8 wherein said high-level language comprises one of the group of: VHDL and Verilog.

11. The method according to Claim 8 wherein said set of faults comprise any of the group of: stuck at zero and stuck at one.

12. The method according to Claim 8 wherein said built-in self-test circuit performs any algorithm of the group comprising: March C+, Checkerboard, March A, March B, Diagonal, and Walking 0/1.

13. An apparatus to verify the performance of a built-in self test circuit for testing embedded memory in an integrated circuit device comprising:

an embedded memory behavior model wherein said embedded memory behavior model comprises a high-level language model;

a built-in self-test circuit model connected to said embedded memory behavior model wherein said built-in self-test circuit model generates input data and address patterns for said embedded memory behavior model, wherein said embedded memory behavior model outputs memory address and data in response to said input data and address patterns, and wherein said memory address and data are compared to said input address and data in said built-in self-test circuit and a fault output is generated if not matching;

a means of introducing a set of faults into said embedded memory behavior model wherein each member of said set of faults

comprises a finite state machine state, a memory address, and a memory data fault;

a means of simulating said embedded memory behavior model and said built-in self-test circuit model; and

a means of comparing the fault diagnosis output of said built-in self-test circuit model and said set of faults to verify the performance of said built-in self-test circuit.

14. The apparatus according to Claim 13 wherein said set of faults comprises an expected faults database file.

15. The apparatus according to Claim 13 wherein said high-level language comprises one of the group of: VHDL and Verilog.

16. The apparatus according to Claim 13 wherein said set of faults comprise any of the group of: stuck at zero and stuck at one.

17. The apparatus according to Claim 13 wherein said built-in self-test circuit model performs any algorithm of the group comprising: March C+, Checkerboard, March A, March B, Diagonal, and Walking 0/1.

18. The apparatus according to Claim 13 further comprising:

a means of scrambling said input data and address patterns prior to input into said embedded memory behavior model; and

a means of de-scrambling said memory address and data prior to said comparing of said input address and data and said memory address and data in said built-in self-test circuit.

19. The apparatus according to Claim 13 further comprising de-scrambling said set of faults prior to comparing said fault output and said set of faults.

20. The apparatus according to Claim 13 wherein said built-in self-test circuit model comprises a register transfer level or gate level design.